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**DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING**

**MODEL EXAM**

**YEAR/SEM : II/ IV MAX. MARKS : 75 Marks**

**SUBJECT CODE : CS T34 SUBJECT NAME : DSD**

**DATE : 19.01.2023** **DURATION : 3Hrs**

**SECTION –A (20 Marks)**

**PART - I (10 x 2 = 20 Marks)**

**Answer all the questions**

1. State consensus theorem?
2. Simplify the Boolean function xy+xz+yz?
3. What is BCD adder and explain binary parallel adder?
4. What is magnitude comparator?
5. What is shift register?.
6. What is latches,hazards?.
7. Define sequential circuit
8. What is the difference between PROM & EPROM.

9. Define error detection?

1. Define FPGA?.
2. Define Asynchronous sequential circuit

**SECTION – B (55 Marks)**

**Part – II (5 x 11 = 55)**

**Answer the questions**

11.Simplify the following expression using k-map

a) F(x,y,z)= Π(1,2,3,6,7)

b) F(x,y,z)= Π(0,1,5,7)

c) F(w,x,y,z) = Π(2,3,12,13,14,15)

**(Or)**

12. Simplify the Boolean function F(A,B,C,D) Πm(0,2,3,6,7,8,10,12,13)

13. a) Explain in detail the 4-bit binary parallel adder

b) Explain in detail about binary multiplier

**(Or)**

14. Explain with the help of a logic diagram the principle of a carry look ahead adder.

15. Describe the design procedure of JK flip-flop and D ?.

**(Or)**

16. Describe in detail about ripple counter/asynchronous counter?

17. Explain in detail mealy and moore models of finite state machine.

**(Or)**

18.What are the hazards? classify hazards explain with suitable example.

19.Implement a combinational circuit in PLA for the following Boolean function F1(A,B,C)=Πm(0,1,3,4,5,6)

F2(A,B,C)=Πm(0,5,6,7,8,9)

**(Or)**

20. Explain with a neat diagram the a) PAL.b) FPGA c) PLD